

# The PennBMBI: Design of a General Purpose Wireless Brain-Machine-Brain Interface System

Xilin Liu, *Student Member, IEEE*, Milin Zhang, *Member, IEEE*, Basheer Subei, Andrew G. Richardson, *Member, IEEE*, Timothy H. Lucas, *Member, IEEE*, and Jan Van der Spiegel, *Fellow, IEEE*

**Abstract**—In this paper, a general purpose wireless Brain-Machine-Brain Interface (BMBI) system is presented. The system integrates four battery-powered wireless devices for the implementation of a closed-loop sensorimotor neural interface, including a neural signal analyzer, a neural stimulator, a body-area sensor node and a graphic user interface implemented on the PC end. The neural signal analyzer features a four channel analog front-end with configurable bandpass filter, gain stage, digitization resolution, and sampling rate. The target frequency band is configurable from EEG to single unit activity. A noise floor of  $4.69 \mu\text{V}_{\text{rms}}$  is achieved over a bandwidth from 0.05 Hz to 6 kHz. Digital filtering, neural feature extraction, spike detection, sensing-stimulating modulation, and compressed sensing measurement are realized in a central processing unit integrated in the analyzer. A flash memory card is also integrated in the analyzer. A 2-channel neural stimulator with a compliance voltage up to  $\pm 12 \text{ V}$  is included. The stimulator is capable of delivering unipolar or bipolar, charge-balanced current pulses with programmable pulse shape, amplitude, width, pulse train frequency and latency. A multi-functional sensor node, including an accelerometer, a temperature sensor, a flexiforce sensor and a general sensor extension port has been designed. A computer interface is designed to monitor, control and configure all aforementioned devices via a wireless link, according to a custom designed communication protocol. Wireless closed-loop operation between the sensory devices, neural stimulator, and neural signal analyzer can be configured. The proposed system was designed to link two sites in the brain, bridging the brain and external hardware, as well as creating new sensory and motor pathways for clinical practice. Bench test and *in vivo* experiments are performed to verify the functions and performances of the system.

**Index Terms**—Brain-Machine-Brain Interface (BMBI), closed-loop BMI, neural recording, neural stimulation.

## I. INTRODUCTION

NEURAL stimulation and recording can be used to communicate bidirectionally between the brain and external hardware. The artificial pathways created by these neural interfaces have shown to be promising in replacing

Manuscript received May 12, 2014; revised August 08, 2014 and October 22, 2014; accepted December 28, 2014. Date of publication March 05, 2015; date of current version April 29, 2015. This work was supported in part by National Institutes of Health grant K12NS080223, National Science Foundation, through grants CBET-1404041 and REU EEC-0754741. This paper was recommended by Associate Editor C. Van Hoof. (*Corresponding author: Milin Zhang.*)

X. Liu, M. Zhang, and J. Van der Spiegel are with the Department of Electrical and Systems Engineering, University of Pennsylvania, Philadelphia, PA 19104 USA (e-mail: zhangmilin@seas.upenn.edu).

B. Subei is with the Department of BioEngineering, University of Illinois at Chicago, Chicago, IL 60607 USA.

A. G. Richardson and T. H. Lucas are with the Department of Neurosurgery, University of Pennsylvania, Philadelphia, PA 19104 USA.

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TBCAS.2015.2392555

sensory and motor pathways lost due to neurological injury or disease [1], [2].

Most existing sensorimotor interfaces are proof-of-concept systems using wired connections and rack-mounted equipment. As the field has matured, researchers have begun to develop electronics to allow neural interfaces to function outside of a laboratory or clinical setting. In normal motor learning, the amount of practice with artificial sensorimotor pathways is directly related to the skill with which the tasks can be performed [3], [4]. Quantifying the performance levels is critical to properly assessing their risk-benefit ratio for clinical translation. Even at the present stage of pre-clinical development, there is a compelling need for portable systems. In addition, including a wireless link between different devices in a BMBI system is essential for the portability of the entire system. Development to date has focused mostly on wireless links for multichannel neural recording and stimulating. However, the implementation of artificial sensorimotor pathways requires devices that can, in real-time, close the loop between recording and stimulating.

Previous closed-loop neural recording and stimulating devices have been designed to link two sites in the brain to create new neural pathways [5], [6] or provide therapeutic stimulation contingent on neural events (e.g., epileptic seizures) [7], [8]. In contrast, our objective is to link the brain to external hardware to create new sensory and motor pathways. In particular, our goals are to design a system i) to communicate sensory information to the brain with sensor-controlled wireless neural stimulation and ii) to communicate motor information to an effector with wireless neural recording and processing. If the effector is the paralyzed arm, the latter would also include peripheral nerve stimulation to reanimate the arm [9]. Importantly, these functions must be tightly integrated for real-time operation and implemented with wireless, energy-efficient microelectronics such that users can learn to use these new communication channels in extended practice sessions and during activities of daily living.

In this paper, we present a wireless Brain-Machine-Brain Interface (BMBI) that is, to our knowledge, the first portable system to provide all the necessary hardware for a closed-loop sensorimotor neural interface. A four-channel analog front-end with high input impedance is designed in this work, recording neural signals from EEG to single unit activity, with the strength of the input signal varying from less than  $1 \mu\text{V}$  to around  $1 \text{ mV}$ , and the frequency band varying from DC to  $10 \text{ kHz}$ . Configurable analog band-pass filters are used to suppress electrode offset, and bandpass the signal in the frequency of interest. An additional programmable gain stage and an analog to digital convertor (ADC) with programmable sampling rate

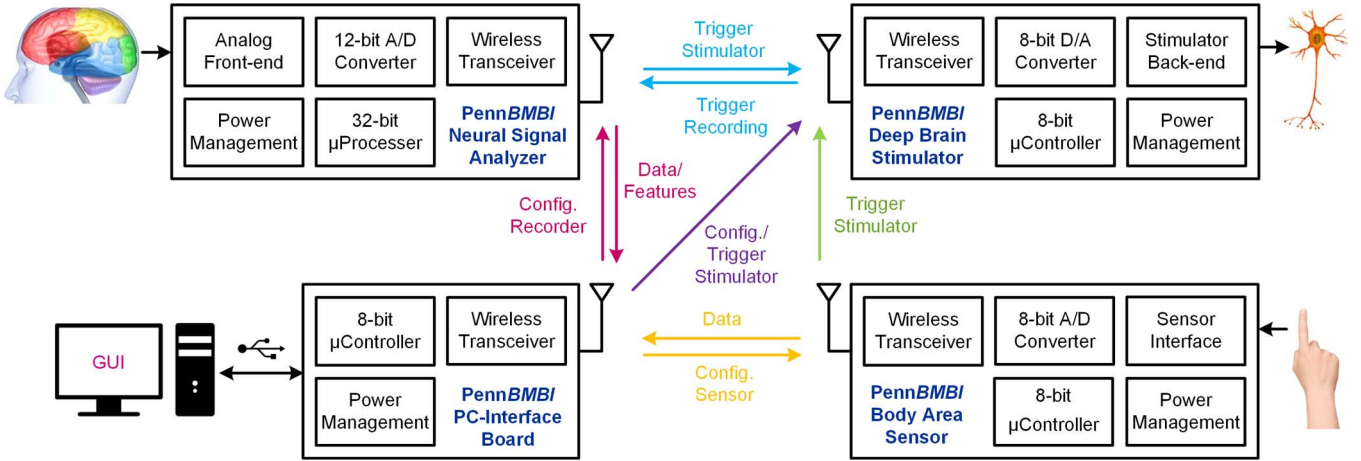


Fig. 1. The BMBI system include four kinds of devices: neural signal analyzer, neural stimulator, body-area sensor node and computer interface. All devices can be configured wirelessly in a computer GUI. Possible closed-loop operation between devices are shown.

and resolution are employed. Digital filtering, neural feature extraction, spike detection, sensing-stimulating modulation, and compressed sensing measurement are realized in a central processing unit integrated on board. The flash memory card is activated in low-power operation mode, for compressed sensing recovery verification, and for data backup. A dual-channel stimulator with high driving capability enables charge-balanced current stimulation up to  $400 \mu\text{A}$  with a compliance voltage of  $\pm 12 \text{ V}$  for functional electrical stimulation. The device can be wirelessly controlled to deliver capacitively coupled current pulses with programmable pulse shape, width, pulse train frequency and latency. In particular, a multi-functional body-area sensor node is included in the system, which enables communication of the sensory information to the brain with sensor-controlled wireless neural stimulation, and also the communication of the motor information to an effector with wireless neural recording and processing. The sensor node integrates a 3-axis accelerometer, a temperature sensor, a flexiforce sensor and a general extension port connected to ADC, which can be used with different commercial sensors, such as pressure sensor, motion sensor, etc. A wireless link is implemented in all the devices for data transfer and on-line configuration through a graphic user interface.

The paper is organized as follows. Section II analyzes the design specification based on the requirements of a general purpose brain-machine-brain system. A customized communication protocol is described in this section according to the specification analysis. Architecture and hardware implementation of all the hardware devices, including the neural signal analyzer, the stimulator and the sensor node, are detailed in the following section. Experimental results include bench tests as well as *in vivo* experiments are presented in Section IV. Section V concludes the paper.

## II. SYSTEM OVERVIEW

### A. Specification Analysis

The goal of a general purpose brain-machine-brain system is to effectively link the brain to external hardware to create new sensory and motor pathways. As illustrated in Fig. 1, four

kinds of devices are required to interface between the brain, the body and the PC, including i) a neural signal analyzer, ii) a deep brain stimulator, iii) a smart sensor node, and iv) a PC interface board with the graphic user interface (GUI). Due to the requirement of portability, the analyzer, the stimulator and the sensor node must be powered either wirelessly or by battery. Different combinations of the devices can be configured depending on the applications. For example, in a recorder-stimulator closed-loop application, the neural signal analyzer is used for neural signal acquisition and processing. The processing results are used to trigger the stimulator. The states of both the neural signal analyzer and the stimulator are monitored and recorded by the GUI wirelessly. In a sensor-stimulator closed-loop application, the sensory information acquired from the sensor node will be analyzed to trigger the stimulator.

In other applications, it requires different neural signal collected from a variety layers of the brain. In order to increase the flexibility of the neural signal analyzer, configurable specifications are applied to the design, enabling signal recording from electrical activity along the scalp to electro-physiological responses of a single neuron. The amplitude of the input signal varies from less than  $1 \mu\text{V}$  to around  $1 \text{ mV}$ . The frequency band of interest varies from DC to  $10 \text{ kHz}$ . Depending on the application, the recorded data will be directly transferred to the PC for off-line data analysis, or be employed to trigger the stimulator after on-line analysis. A band pass filter is employed to filter out the frequency range of interest. The cutoff frequencies and gain of the high-input impedance filter can be configured from the GUI through wireless link. An on-line data analysis unit is implemented for neural feature extraction, spike detection, sensing-stimulating modulation and/or compressed sensing.

The smart sensor node provides the system with an additional biological signal input. The purpose of the sensor node is two-folded: i) to reconstruct sensory information mimicking receptor cells located on human skin, ii) to monitor environmental changes and/or body movement. Various sensing capabilities, including pressure, vibration and temperature, can be integrated onto the sensor node. The weight and volume is significant to realize a wearable sensor node. The sensory data will

TABLE I  
A COMPARISON BETWEEN VARIOUS BRAIN-COMPUTER-INTERFACE SYSTEM  
PROPOSED IN LITERATURE

	Recorder	Stimulator	Sensor	Wireless	Portability
[5]	PCB <sup>†</sup>	PCB	IMU	N/A	Yes
[6]	CMOS 0.35 $\mu$ m	CMOS 0.35 $\mu$ m	N/A	N/A	Yes
[8]	Commercial <sup>‡</sup>	Commercial	IMU	N/A	No
[10]	PCB	PCB	N/A	N/A	No
[12]	CMOS 180nm	N/A	N/A	CMOS 180nm	Yes
[13]	CMOS 65nm	N/A	N/A	CMOS 65nm	Yes
[14]	CMOS 180nm	CMOS 180nm	N/A	N/A	Yes
[15]	CMOS 180nm	CMOS 180nm	N/A	CMOS 180nm	Yes
[16]	CMOS 130nm	N/A	N/A	CMOS 130nm	Yes
[17]	PCB	PCB	N/A	Zigbee	Yes
[18]	CMOS 0.35 $\mu$ m	CMOS 0.35 $\mu$ m	N/A	N/A	Yes
[19]	Commercial	PCB	N/A	N/A	No
[20]	Commercial	Commercial	Camera	N/A	No
This work	PCB	PCB	Multiple	Yes	Yes

<sup>†</sup> "PCB" indicates designs with off-the-shelf components for the implementation of the function.

<sup>‡</sup> "Commercial" indicates designs with commercial available single-chip solution for either the analog front end of the recorder or back end of the stimulator.

be either sent back to the PC for off-line processing, or be directly employed to trigger the stimulator.

The requirement of the driving capability of the stimulator varies with the application. The stimulator can be wirelessly triggered through i) the GUI, ii) the neural signal analyzer, and iii) the smart sensor node, depending on the applications.

Table I compares the proposed work with similar designs in the literature. From the comparison, we can see that previous closed-loop neural recording and stimulating devices were designed to link two sites in the brain using neural-activity-dependent stimulation to create new neural pathways [5], [6]. In contrast, our device links the brain to external hardware to create new sensory and motor pathways. In addition, the wireless module is applied to all the devices in our system, which greatly increase the system portability.

### B. Wireless Communication Protocol Design

The proposed system is developed using off-the-shelf components, enabling reliable, low cost, fast prototype implementation for various experimental applications in brain-machine-brain interface research. Wireless links have been built between all devices for configuration, data transfer and closed-loop operation. The transceivers nRF24L01+ from Nordic Semiconductor [31] is employed in the system, which features a maximum on-the-air data rate of 2 Mbps in 2.4 GHz ISM band using GFSK modulation. Embedded Enhanced ShockBurst baseband protocol engine and automatic packet transaction handling are integrated in the transceiver. Commands and data were sent with two-byte Cyclic Redundancy Check (CRC) scheme and

TABLE II  
ORGANIZATION OF THE MEMORY BANK

Bank Addr	Word Addr	Description	Value
BANK 00	word 00	Password	
BANK 01	word 00 bit[1:0]	ID - Property	00 - GUI 01 - Neural analyzer 10 - Stimulator 11 - Sensor node
	word 00 bit[7:2]	ID - Serial #	0x00 - 0x3F
BANK 10	word 00	Bank 10 Length	
	word 01	Bank 11 Length	
	word 10-END	Configuration	
BANK 11	word 00-END	User memory	

an auto-retransmit with acknowledgement ability. A communication distance of 3 meters is achieved with a data loss of less than 0.05% under 2 Mbps transmission rate, which satisfies the requirement of body area *in-vivo* experiment.

A customized protocol has been designed for communication with all the devices in the system to avoid on-the-air conflicts. The four devices are divided into two classes as 1) central unit, which is realized in the PC through an interface device; and 2) satellite devices, including the analyzers, the stimulators and the sensor nodes. The memory in each satellite device is organized in 4 banks, consisting of 8-bit words as illustrated in Table II. A password is saved in Bank 00 for kill and/or lock functions. Bank 01 is reserved for device ID number and class identity. Bank 10 records all the configuration information for on-line processing. Bank 11 is user memory which can be freely organized in any fashion depending on the application.

All the satellite devices can be configured by the central unit via the wireless communication channel. The commands are all organized in a "header + argument + data" format. Acknowledge information from the slave devices is also organized in the same format. A list of all the available commands used for communication between devices are listed in Appendix A.

A PC interface board with high speed USB 2.0, and a Matlab based graphic user interface (GUI), as illustrated in Fig. 2, have been built for wireless monitoring, controlling and configuring all devices. Closed-loop operation can also be easily configured in the GUI. All the devices receive interprets and commands from the PC GUI and talk to the target device through corresponding channel/address via a wireless link. There are six major panels of the GUI, including: 1) PC configuration panel, where the communication port can be configured. All the configurations (including other panels) can be exported or loaded; 2) analyzer configuration panel, where the gain, sampling rate/resolution, filter pass-band can be configured for each individual channel. For the signal processing modes performed in hardware, the time window size and threshold for spike detection can also be configured; 3) stimulator configuration panel, where the amplitude, pulse width, pulse train number, and time interval of the stimuli can be configured; 4) body-area sensors configuration, where parameters for sensor nodes can be configured; 5) closed-loop configuration, where closed-loop operation between different devices can be configured; 6) display windows, where output from analyzers and sensor nodes can be displayed in real time.

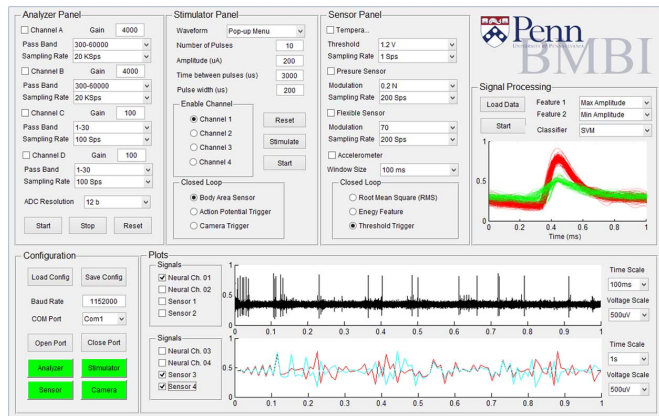


Fig. 2. Matlab based Graphical User Interface (GUI). Six major panels are included in the GUI, which are: 1) PC configuration; 2) recording device configuration; 3) stimulator configuration; 4) body-area sensors configuration; 5) closed-loop configuration; 6) display windows.

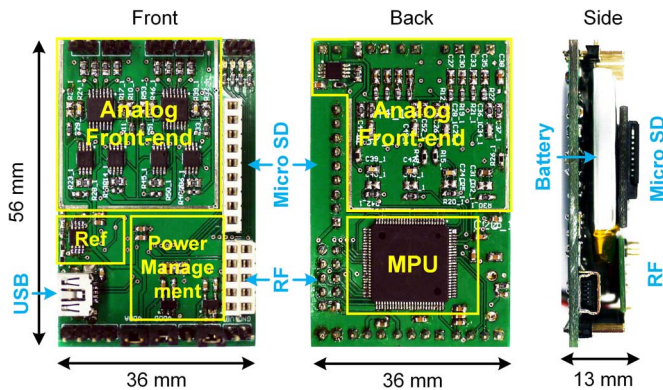


Fig. 3. Photograph of the PennBMBI neural signal analyzer (NSA) in front, back and side view. The wireless module and MicroSD card is not shown in the front view.

### III. ARCHITECTURE AND HARDWARE IMPLEMENTATION

#### A. Neural Signal Analyzer

A Neural Signal Analyzer (NSA), with a size of 56 mm  $\times$  36 mm  $\times$  13 mm, is designed to perform general neurological signal recording and analysis, as shown in Fig. 3. The NSA integrates a four-channel analog front-end, a central processing unit (CPU), a 2.4 GHz wireless transceiver, a removable MicroSD card, a power management unit, and other peripheral circuits. An extension board holding the MicroSD socket can be plugged in through the connector as shown in the front and back view when necessary.

The analog front-end integrates four independent amplifier channels, sharing a tissue ground driving circuit. The architecture of the front-end circuit is shown in Fig. 4. A supply voltage of 3.3 V is used. The common mode voltage is set to be 1 V. Configurable gain stages and filters are designed in order to meet the requirement of recording neurological signals with different bandwidth and signal levels [22]. The differential input signal is AC coupled to the instrumentation amplifier with a high input impedance and a corner frequency of 0.5 Hz. This is compatible with standard high impedance electrodes and removes the DC offset resulting from the electrode polarization. The gain of the

instrumentation amplifier is fixed at 200, with a bandwidth of 12.5 kHz [23]. Resistors with low temperature coefficient (TC) are used to minimize gain drift. An integrator implemented by amplifier A4 (Fig. 4) with configurable capacitor is used as a high pass filter. Amplifier A5 is used to provide an additional gain stage with configurable low pass filter.

An Atmel 32-bit AVR Microcontroller AT32UC3C1512C [25] is implemented in the NSA. The MCU integrates a 12-bit pipeline ADC with a multiplexer, S/H circuits and a programmable gain stage. A programmable gain ranging from 46 dB to 102 dB in total is achieved in the NSA. In the recording mode, a peripheral direct memory access (DMA) controller is used for digital data acquisition, data buffering, and serial peripheral interface (SPI) accessing. Captured signals can be sent out via the wireless module or to the MicroSD card through SPI. The DMA handshakes with peripheral interfaces directly, while the central processor core is in the sleep mode to save power.

On-line neural signal processing is performed in the 32-bit floating point DSP core in the MCU. Various function blocks are built, including,

- 1) Digital bandpass filter. Type-I real Finite Impulse Response (FIR) filter is used as bandpass filter. Six frequency bands are pre-defined, and the filter coefficients with 24 taps and 10 taps are pre-written in the flash memory for different filtering requirements.
- 2) Time-domain feature extractor. Common time-domain features, such as line-length, area, energy, maximum/minimum, and zero-crossing, are extracted in real-time by a proper configuration of the sliding window length and overlay.
- 3) Spectral energy feature extractor. 16/128-point FFT is used for spectral analysis.
- 4) Compressed sensing measurement. Neural signal features sparsity in certain basis/dictionaries [27], enabling a near lossless reconstruction under sub-Nyquist sampling. A signal agnostic compressed sensing measurement is implemented in the CPU. The input signal vector length  $N$  is set to be 512, and the measurement number  $M$  ( $M < N$ ) can be programmable to 256, 128, 64, or 32.  $y = \Phi x$  is realized as the compressed sensing measurement, where  $x \in \mathbb{R}^{N \times 1}$  is the input neural signal,  $y \in \mathbb{R}^{M \times 1}$  is the measurements, and  $\Phi \in \mathbb{R}^{M \times N}$  is the measurement matrixes. Pseudo random projection stored in the flash memory is used for the implementation of  $\Phi$ . The reconstruction is performed on the receiver end using a convex optimization algorithm.
- 5) Action potential detection. The filters are configured to first extract signals in the band of 300 to 6 kHz. An amplitude threshold  $S_{th}$  is set for a rough unsupervised spike sorting for input signals in the frequency band of 300 to 6 kHz. The value of  $S_{th}$  is four-times the estimation of the standard deviation of the background noise. Two time-amplitude windows are open to perform discrimination of the action potentials after the input signal cross the threshold with a positive derivative.

The NSA wireless transceiver can be configured to different operation modes, sending recorded raw data, neural features,

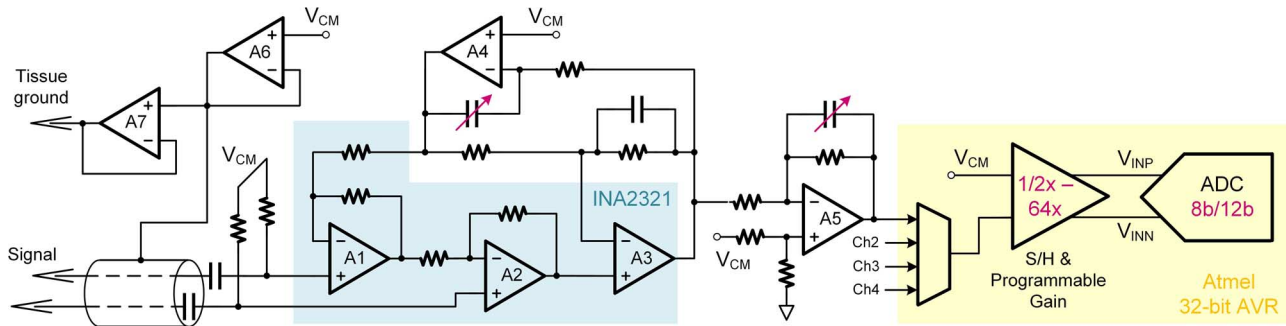


Fig. 4. Architecture of the analog front-end.  $V_{CM}$  is the common mode voltage. A1~A4 forms the instrumentation amplifier with high pass filter. A5 works as the second gain stage with configurable gain and low pass filter. The third gain stage has programmable gain. The ADC digitize the amplified neural signals at configurable sampling rates and resolution. A6 and A7 are shared by the four channels to drive the shield potential and tissue ground.

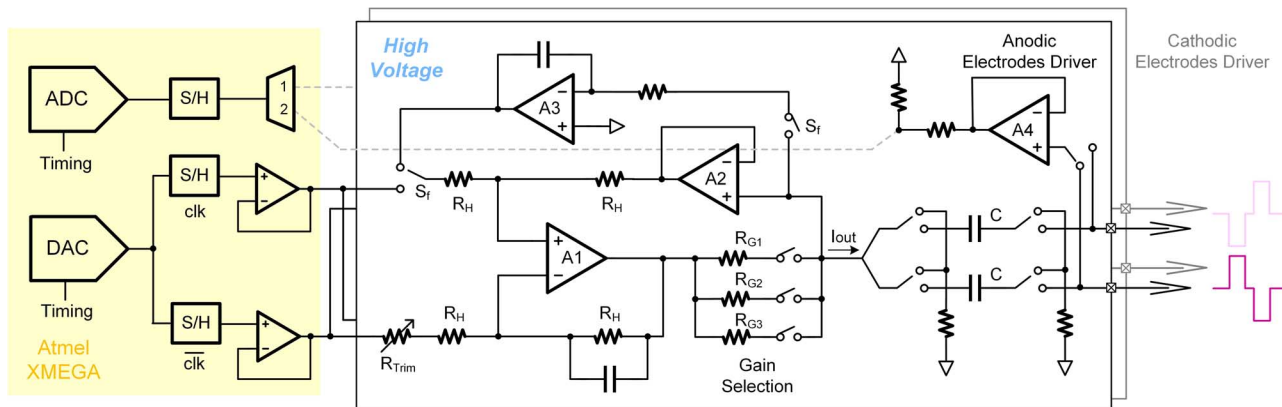


Fig. 5. Circuit schematic of the high compliance voltage current source output stage. Arbitrary stimuli waveform is generated by digital to analog converter. V-to-I gain is programmable to provide high dynamic range.

spike time stamps, or compressed sensing measurements to the GUI, respectively. It also enables the sending of mapped stimuli patterns to the stimulating device, or receive triggers for recording from other devices.

The NSA is powered by a rechargeable 3.7 V lithium-ion battery (Ultralife UBPO02). A supply voltage of 3.3 V is used for the analog front-end, digital micro-controller and wireless transceiver. The quiescent current of the analog front-end is 380  $\mu$ A per channel. The CPU consumes 490  $\mu$ A per MHz. The 950 mAh battery supports the device for overnight continuous recording.

### B. Neural Stimulators

A dual-channel neural stimulator with a size of 43 mm  $\times$  27 mm  $\times$  8 mm, as illustrated in Fig. 6, is designed to deliver bipolar or unipolar, charge-balanced current pulses with programmable pulse shape, amplitude, width, pulse train frequency and latency. The stimulator integrates a current driving back-end, a microcontroller (MCU) integrated DAC and ADC, a wireless transceiver, a power management unit, and other peripheral circuits.

A dual DC-DC converter is used for boosting the voltage from a 3.7 V lithium-ion battery to  $\pm$ 12 V to drive the output

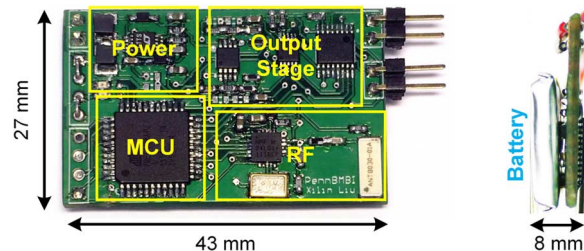


Fig. 6. Photograph of the neural stimulator. The stimulator includes a current driving back-end, a MCU integrated DAC and ADC, a wireless transceiver, a power management unit.

current stage, in order to provide a sufficient compliance voltage for stimulating through high impedance electrodes. The converter will be switched to idle mode when no stimulation is to be delivered in order to reduce power consumption. A modified Howland current source is employed as bi-directional current driving stage, as illustrated in Fig. 5. Amplifiers A1 to A4 are implemented using high-voltage dual supply op-amps with JFET inputs. A resistor trimmer is used to trim the equal-value resistor network to achieve good common mode rejection ratio (CMRR) and high output impedance from the Howland current source. A feedback capacitor is added for stability. Different

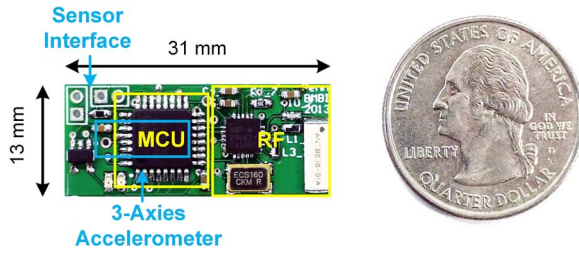


Fig. 7. The photograph of sensor node in comparison with a quarter.

TABLE III  
POWER CONSUMPTION OF THE SENSOR NODE

Microcontroller	240 $\mu$ A	Accelerometer [30]	23 $\mu$ A
RF Sleep [31]	0.9 $\mu$ A	Thermistor	< 7 $\mu$ A
RF Transmit	7 mA	Flexiforce sensor	< 50 $\mu$ A
Total Working	321 $\mu$ A	Total Transmit	7.3 mA

transconductances can be selected by setting the gain resistors in order to get a large dynamic range. Amplifier A2 is a unity-gain buffer used to reduce the requirement for calibration under different gain settings. A feedback integrator, A3, is used in idle mode to improve the stability as well as to reduce the current leakage [5]. Amplifier A4 is implemented for buffering the electrode potential, and the impedance of the electrode is calculated in the MCU. A low impedance threshold is set to stop stimulating in case of electrode shorting. In addition, a blocking capacitor is used in each channel to prevent direct current injection and limits the maximum net charges.

The two channels are used as differential input of the Howland current source to minimize the offset. The DAC is shut down and both inputs are grounded in idle mode to reduce power consumption. The ADC is triggered twice during the stimulation phase to estimate the compliance voltage on the electrode, as well as to evaluate the impedance. If the electrode impedance is lower than a user-defined threshold, all the stimulation will be stopped and an alert will be sent to computer.

### C. Body Area Sensors

The multi-functional body area sensor node features a size of 31 mm  $\times$  13 mm  $\times$  8 mm, as shown in Fig. 7. The sensor node integrates a microcontroller, a 3-axis digital accelerometer, a temperature sensor, and a flexiforce sensor.

The accelerometer interfaces with the MCU through I2C protocol. The outputs of the thermistor and the flexiforce sensor outputs are analog, which are digitized using an 8-bit SAR ADC integrated in the MCU. General purpose ports are saved for up to 12-channel potential extensions of the sensor node. The sensor node is powered by a 2.65 g, 110 mAh rechargeable lithium battery. The power consumption of all the modules used in the sensor node is listed in Table III.

## IV. EXPERIMENTAL RESULTS

### A. Bench Testing

Fig. 8 shows the measured input referred noise spectrum of the analog front-end in the neural signal analyzer. The integrated noise is 4.69  $\mu$ V<sub>rms</sub> in the wide band. The noise efficiency factor [32] is 14.6. The mid-band gain error is 0.87%

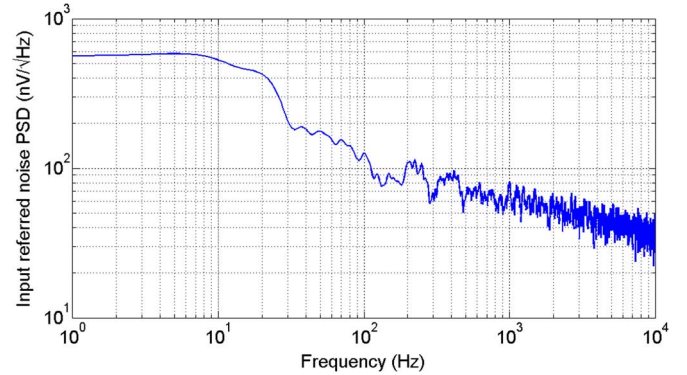


Fig. 8. Input referred noise spectrum of the analog front-end.

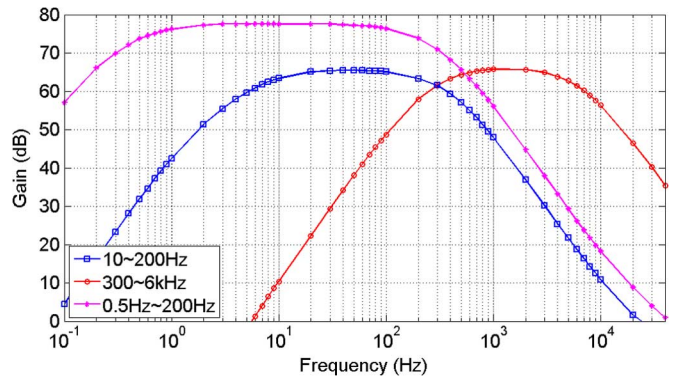


Fig. 9. The measured frequency response of the analog front-end in different configurations. (blue) 10 to 200 Hz with a gain of 66 dB, (red) 300 to 6 kHz with a gain of 66 dB, (magenta) 10 to 200 Hz with a gain of 78 dB.

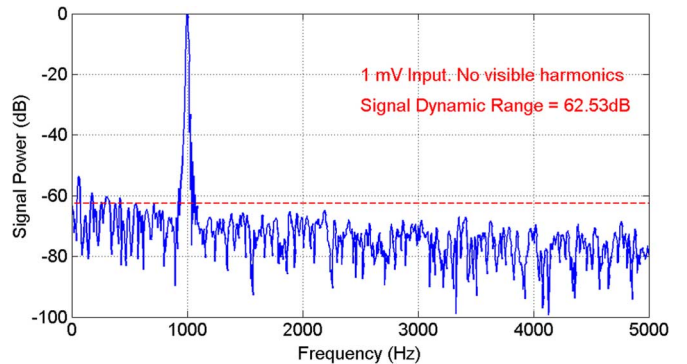


Fig. 10. Dynamic range of the signal. Input signal is 1 mV at 1 kHz.

and the measured CMRR at 1 kHz is 67.4 dB. The measured frequency response in different configurations are shown in Fig. 9. The dynamic range of the analog front-end is measured with an 1 mV peak-to-peak amplitude input signal at 1 kHz, as illustrated in Fig. 10. Different bandpass filters with different gain are applied, e.g., 10 to 200 Hz with a gain of 66 dB, 300 to 6 kHz with a gain of 66 dB, and 10 to 200 Hz with a gain of 78 dB. The characteristics of the neural signal analyzer is summarised in Table IV.

The output currents of the neural stimulator is measured under different loads. Fig. 11(a) shows the standard deviation of the output current of anodic and cathodic drivers across the different loads. The standard deviation is calculated for

TABLE IV  
SPECIFICATIONS OF THE PENNBMBI SYSTEM

Neural Signal Analyzer			
Supply voltage	3.3V	Supply current	380 $\mu$ A/ch
Input Impedance	>200M $\Omega$	Offset tolerance	1V
I-Amp Noise floor	4.69 $\mu$ Vrms	I-Amp CMRR	>61dB
ADC resolution	12 bit		
Neural Stimulator			
Output current	0 ~ 1mA	DAC resolution	6 bit
Compliance voltage	$\pm$ 12V	Output impedance	> 100M $\Omega$
Standard deviation	1.71 $\mu$ A	Driver mismatch	0.75%

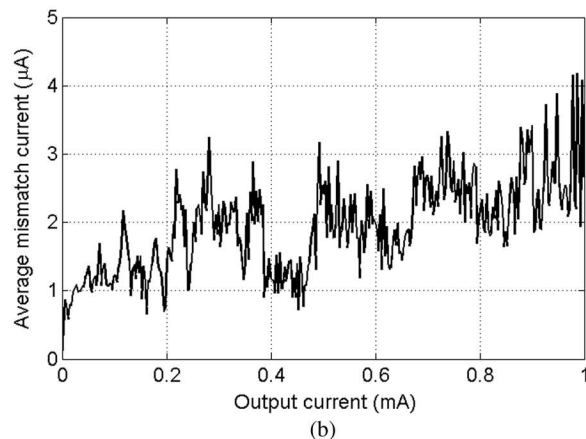
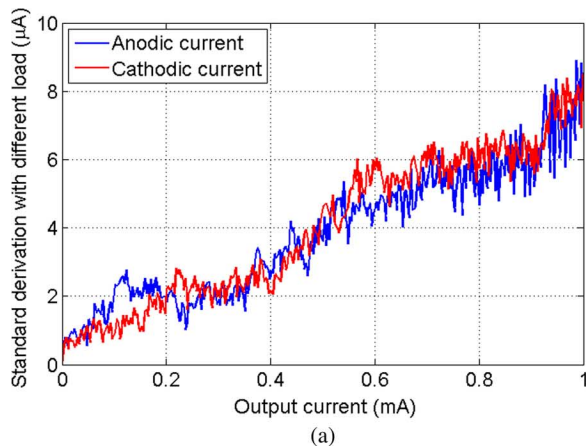


Fig. 11. The measured output current for different load (1 k $\Omega$ , 2 k $\Omega$ , ..., 8 k $\Omega$ ). (a) Shows the standard deviation of the output current across different loads. (b) Shows the average current mismatch between anodic and cathodic electrodes across different loads.

each output current with all the different loads. The average of the calculated standard deviation for different currents in the output stage is 3.91  $\mu$ A. Fig. 11(b) shows the average current mismatch between the anodic and cathodic electrodes across different loads. The average mismatch with respect to the corresponding output current is 0.75%. The stimulator is also tested in 0.9 g/100 mil Sodium Chloride using a 75  $\mu$ m tungsten electrode. Fig. 12 shows the measured voltage across the bipolar electrodes for different stimulation current levels. A blocking capacitor of 1  $\mu$ F is used.

A lower than  $10^{-3}$  bit error rate (BER) is measured in the wireless module for a distance of 3 m in a normal animal experiment environment.

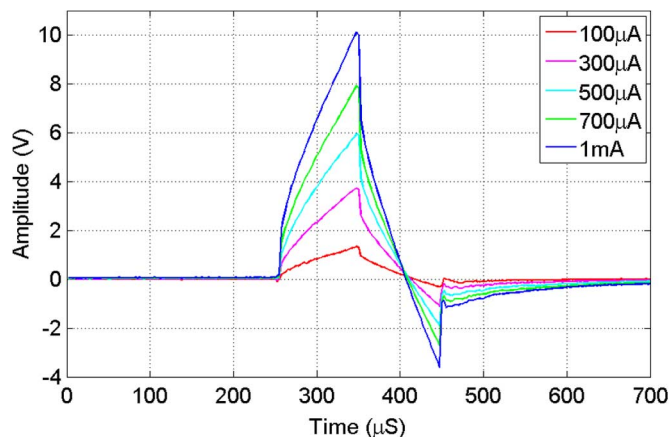


Fig. 12. Measured different stimulation pulses in sodium chloride solution.

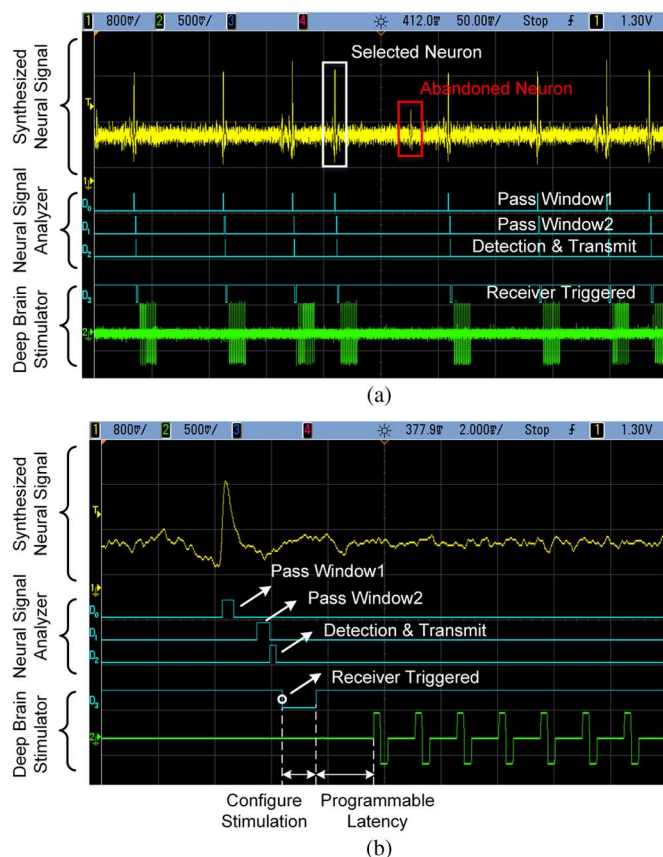


Fig. 13. Measured wireless closed-loop operation from neural signal analyzer and deep brain stimulator. Zoomed-in view of (a) is shown in (b).

Two open-loop experiments have been performed to verify the system level operation. In the first experiment, the NSA to stimulator pathway is tested. As shown in Fig. 13(a), neural signal is first captured by the NSA. On-board AP detection is performed using a dual threshold comparison methods. A pass window is generated when the input signal cross the threshold. An AP is denoted when two pass windows are detected. Once an AP is detected, as shown in the zoomed-in view in Fig. 13(b), a CMD CFG is wirelessly sent from the NSA to the stimulator, triggering a group of pulse stimulations. In the second experiment, the sensor to stimulator pathway is tested. As shown in



Fig. 14. Measured wireless closed-loop operation from sensor node and deep brain stimulator.

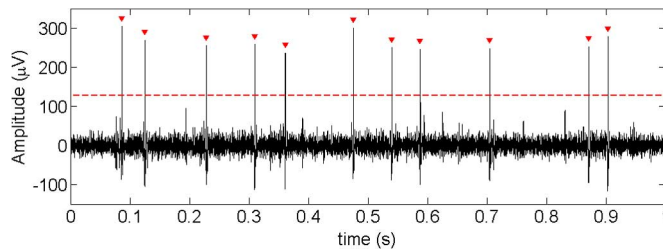


Fig. 15. Action potentials recorded by the neural signal analyzer. Detected spikes are marked by red triangles.

Fig. 14, the amplitude of the sensing result is encoded into the frequency of the pulses generated from the stimulator. A CMD CFG command is wirelessly continuously sent to the stimulator from the sensor node. The argument is encoded according to the digitized sensory output of the sensor node.

### B. In Vivo Testing

To further evaluate the PennBMBI, we performed several basic tests of the wireless neural recording, stimulating and sensing functions in both anesthetized and awake rats. Neural recording was performed in an anesthetized rat with a tungsten microelectrode placed in the whisker motor cortex. The analyzer was configured to have a passband of 300~6 KHz, a sampling rate of 21 KSps, and a gain of 72 dB. The recorded action potentials (APs) are shown in Fig. 15. The results show that the neural signal analyzer faithfully recorded the APs with a signal-to-noise ratio comparable to a commercial system.

In order to evaluate the quality of the captured data, the neural signal was simultaneously recorded by a rack-mounted commercial system (RZ2 Workstation, Tucker-Davis Technologies). A comparison of the signals recorded by the two systems is shown in Fig. 16. The recording shows two different neurons firing APs in close succession.

A cluster analysis is performed on the APs recording by the PennBMBI analyzer. During the experiment, stereotyped AP waveform shape is captured from two neurons at the same time. Normalized maximum and minimum amplitudes are calculated and used as two features for the analysis. Fig. 17(a) illustrates the analysis results in the feature domain, which clearly separates the input signals into two cluster. The raw AP is labelled with different colors according to the classification results, as shown Fig. 17(b).

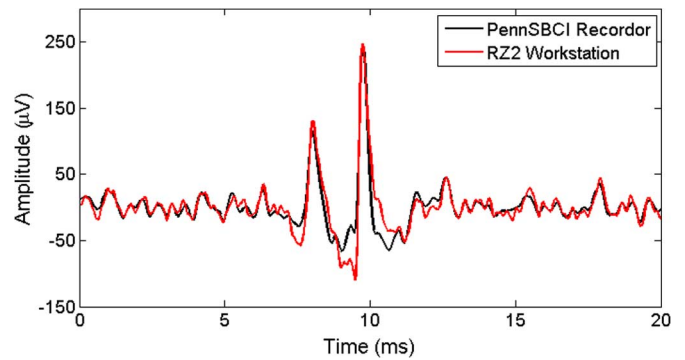


Fig. 16. Comparison between data captured by the PennBMBI analyzer (black) and RZ2 neurophysiology workstation (red).

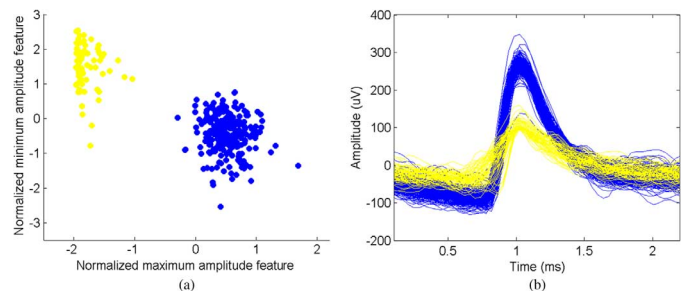


Fig. 17. A cluster analysis of the APs recorded by the PennBMBI analyzer. (a) Normalized maximum and minimum amplitudes are calculated and used as two features for the analysis. (b) The raw AP is labelled with different color according to the classification results.

To demonstrate the sensor and stimulator nodes, an awake rat with a chronically implanted stimulating microelectrode in the lateral hypothalamus was placed in an operant conditioning chamber with a lever press. The sensor node detected the lever press and wirelessly sent a trigger to the stimulator worn on the rat's back to deliver a stimulus train (30 100  $\mu$ A, 200  $\mu$ s constant current pulses) to the microelectrode. This setup allowed the rat to associate the lever press with the rewarding sensation of hypothalamic stimulation. This result provides one example of how the various nodes of the PennBMBI, in this case the sensor and stimulator, can be flexibly combined to enable a wide range of neuroscience and neuroengineering experiments in freely behaving animals.

## V. CONCLUSION

This paper describes a portable wireless Brain-Machine-Brain Interface (BMBI) that links the brain to external hardware, establishing sensory and motor pathways. Four modules are included: i) neural signal analyzer, ii) neural stimulators, iii) multiple sensor nodes, and iv) PC interface. All the devices can be wirelessly configured through a graphic user interface on the PC. The four devices can be used together or separately depending on the applications. A performance summary of the proposed design as well as a comparison with reported results in the literature is listed in Table V. Both multi-channel neural recording front-ends and neural stimulators have been proposed in literature and widely used in different applications including the one described in this paper. The systems described in some of the recent papers



TABLE V  
SYSTEM SUMMARY AND COMPARISON TO CLOSED-LOOP BMBI

Features	Zanos <i>et al</i> [5]	Azin <i>et al</i> [6]	Gao <i>et al</i> [16]	Borton <i>et al</i> [12]	Nguyen <i>et al</i> [10]	This Work
Year	2011	2011	2012	2013	2013	2013
Recording front-end	3 unipolar/bipolar	4 bipolar	96 unipolar	100 unipolar	32 bipolar	4 unipolar/bipolar
Adjustable gain/filter	Yes	Yes	No	No	Yes	Yes
Signal processing	Spike detection	Spike detection	N/A	N/A	Spike sorting	Spike detection Feature extraction Compressed sensing
Stimulation back-end	3 unipolar/bipolar	4 bipolar	N/A	N/A	Optical stimuli	6 & 2 unipolar/bipolar
Body-area sensors	Accelerometer	N/A	N/A	N/A	N/A	Accelerometer Pressure sensor Temperature sensor
Wireless link	N/A	N/A	30 Mbps	24 Mbps	N/A	2 Mbps
Flash memory	Yes	N/A	N/A	N/A	N/A	Yes
Graphic user interface	Yes	N/A	N/A	N/A	Yes	Yes
Closed-loop operation	Recording -Stimulating	Recording -Stimulating	No	No	Recording -Stimulating	Recording-Stimulating Sensor-Stimulating

incorporate also a low-power wireless link. However, for the application using a large scale electrode array, the requirement of the transmission rate of the wireless module increases, which will result in an increasing of the power consumption. In order to reduce the amount of data for data transmission, different on-board, real-time neural signal processing have been proposed in literature, such as filtering and spike detection. The work described in this paper adds also compressed sensing, which allows a sampling rate lower than Nyquist rate without a significant sacrificing of the quality of the signal. As a general purpose platform, this work includes all the required devices for building an artificial neural pathway from the brain to the body. The wireless module implemented in all the devices of this work greatly improve the portability of the devices. The additional on-board memory provides an option for long term, high quality data acquisition. Different neural signal processing modules have been implemented in the NSA, which can be remotely selected through the GUI. Bench tests evaluate the performance of the proposed system. *In vivo* experiments illustrate a close-loop application of the system. Future tests will focus on demonstrating the intended therapeutic function of the PennBMBI, namely, linking the brain to external hardware to create new sensory and motor pathways.

#### APPENDIX A COMMUNICATION COMMANDS

Table VI illustrates all the available commands used in the system for communication between devices. The commands are all organized in a “header + argument + data” format, including (priority from high to low).

1) CMD RST. Reset command includes global reset command and local reset command. Global reset command terminates all the undergoing procedure in all the devices in the system, while a local reset command only works on selected devices with a matched ID in the header. Global reset command can only be sent by the central unit, while local reset command can be sent from any host device. Acknowledge from the slave will report the state before the reset operation. The slave device will enter IDLE state after the reset operation.

TABLE VI  
ORGANIZATION OF THE CUSTOMIZED COMMUNICATION COMMAND

CMD RST †	Header	CMD ID, 8bit
		Host ID, 8bit
		Client ID, 8bit (0x00 for global reset)
ACK RST	Header	ACK ID, 8bit
		Device ID, 8bit
	Argument	STATE ID
CMD STD	Header	CMD ID, 8bit
		Host ID, 8bit
		Client ID, 8bit (0x00 for global pause)
ACK STD	Header	ACK ID, 8bit
		Device ID, 8bit
	Argument	STATE ID
CMD WKP	Header	CMD ID, 8bit
		Host ID, 8bit
		Client ID, 8bit (0x00 for global wake-up)
ACK WKP	Header	ACK ID, 8bit
		Device ID, 8bit
	Argument	STATE ID
CMD CFG	Header	CMD ID, 8bit
		Host ID, 8bit
		Client ID, 8bit
Argument (Analyzer)	Channel #, gain, stop frequency 1, stop frequency 2, filter gain, and CRC, all 8bit format	
	Argument (Stimulator)	Channel #, pulses #, pulse width, stimulation/reversal amplitude, stimulation/interphasic/interval time, pulse shape, and CRC, all 8bit format
ACK CFG	Header	ACK ID, 8bit
		Device ID, 8bit
	Argument	STATE ID, 8bit Flag, 0x01 for configuration success
CMD ACC	Header	CMD ID, 8bit
		Host ID, 8bit
		Client ID, 8bit
ACK ACC	Header	ACK ID, 8bit
		Device ID, 8bit
	Argument	Flag, 0x01 for approval
CMD DTX	Header	CMD ID, 8bit
		Host ID, 8bit
		Client ID, 8bit
Data	Repackaged memorized data	
ACK DTX	Header	ACK ID, 8bit
		Device ID, 8bit
	Argument	Flag, 0x01 for successful transmission client device will resend package if failed

† Argument section and data section are not required in CMD RST.

2) CMD STD. Standby command is similar to reset command. It pauses the undergoing procedure in a target de-

vice without reset it. Acknowledge from the slave will report the state it stops at.

- 3) CMD WKP. Wake-up command is used to return a device from IDLE state or to continue a current procedure which was previously stopped by a standby command.
- 4) CMD CFG. Configure command is used for on-line configuration of a target device. The specifications will be embedded in the argument section. The translation of the argument value varies while a different target device is applied. Table VI only list the argument section for the configuration of the analyzer and the stimulator.
- 5) CMD ACC. Access command is a request to get communication channel access. Usually data transfer is followed by this command after a proper acknowledgement is received. Any device with an approved flag received from an acknowledge and the host of the acknowledgement are denoted as a “matched pair”. The transmitting device is defined as client device, while the receiving device is defined as host device.
- 6) CMD DTX. Data transmission command is not a real command. It carries the repackaged memorized data from a matched client device to a matched host device.

#### ACKNOWLEDGMENT

The authors would like to thank P. Weigand for help with collecting the data.

#### REFERENCES

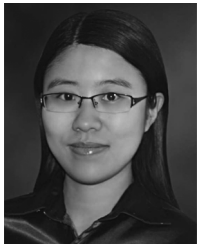
- [1] L. R. Hochberg *et al.*, “Reach and grasp by people with tetraplegia using a neurally controlled robotic arm,” *Nature*, vol. 485, pp. 372–375, 2012.
- [2] J. E. O’Doherty *et al.*, “Active tactile exploration using a brain-machine-brain interface,” *Nature*, vol. 479, pp. 228–231, 2011.
- [3] K. Ganguly and J. M. Carmena, “Emergence of a stable cortical map for neuroprosthetic control,” *PLOS Biol.*, vol. 7, p. e1000153, 2009.
- [4] A. C. Koralek, X. Jin, J. D. Long, R. M. Costa, and J. M. Carmena, “Corticostriatal plasticity is necessary for learning intentional neuroprosthetic skills,” *Nature*, vol. 483, pp. 331–335, 2012.
- [5] S. Zanos, A. G. Richardson, L. Shupe, F. P. Miles, and E. E. Fetz, “The Neurochip-2: An autonomous head-fixed computer for recording and stimulating in freely behaving monkeys,” *IEEE Trans. Neural Syst. Rehabil. Eng.*, vol. 19, no. 4, pp. 427–435, Aug. 2011.
- [6] M. Azin, S. Member, D. J. Guggenmos, S. Barbay, and R. J. Nudo, I. T. Activity-dependent, “A battery-powered activity-dependent intracortical microstimulation IC for brain-machine-brain interface,” *J. Solid-State Circuits*, vol. 46, no. 4, pp. 731–745, 2011.
- [7] M. T. Salam, M. Mirzaei, M. S. Ly, D. K. Nguyen, and M. Sawan, “An implantable closedloop asynchronous drug delivery system for the treatment of refractory epilepsy,” *IEEE Trans. Neural Syst. Rehabil. Eng.*, vol. 20, pp. 432–442, 2012.
- [8] S. Stanslaski, P. Afshar, P. Cong, J. Giftakis, P. Stypulkowski, D. Carlson, D. Linde, D. Ullestad, A.-T. Avestruz, and T. Denison, “Design and validation of a fully implantable, chronic, closed-loop neuromodulation device with concurrent sensing and stimulation,” *IEEE Trans. Neural Syst. Rehabil. Eng.*, vol. 20, no. 4, pp. 410–421, Jul. 2012.
- [9] C. Ethier, E. R. Oby, M. J. Bauman, and L. E. Miller, “Restoration of grasp following paralysis through brain-controlled stimulation of muscles,” *Nature*, vol. 485, pp. 368–371, 2012.
- [10] T. K. T. Nguyen, Z. Navratilova, H. Cabral, L. Wang, G. Gielen, F. P. Battaglia, and C. Bartic, “Closed-loop optical neural stimulation based on a 32-channel low-noise recording system with online spike sorting,” *J. Neural Eng.*, vol. 11, no. 4, p. 046005, Jun. 2014.
- [11] B. Thurgood, D. Warren, N. M. Ledbetter, G. A. Clark, and R. R. Harrison, “A wireless integrated circuit for 100-channel charge-balanced neural stimulation,” *IEEE Trans. Biomed. Circuits Syst.*, vol. 3, no. 6, pp. 405–414, 2009.
- [12] D. A. Borton, M. Yin, J. Aceros, and A. Nurmikko, “An implantable wireless neural interface for recording cortical circuit dynamics in moving primates,” *J. Neural Eng.*, vol. 10, no. 2, p. 026010, Feb. 2013.
- [13] R. Muller, L. Hanh-Phuc, L. Wen, P. Ledochowitsch, S. Gambini, T. Bjorninen, A. Koralek, J. M. Carmena, M. M. Maharbiz, E. Alon, and J. M. Rabaey, “A miniaturized 64-channel 225uW wireless electrocorticographic neural sensor,” in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2014.
- [14] U. Bihl, T. Ungru, H. Xu, J. Anders, J. Becker, and M. Ortmanns, “A bidirectional neural interface with a HV stimulator and a LV neural amplifier,” in *Proc. IEEE Int. Symp. Circuits and Systems*, May 2013, pp. 401–404.
- [15] K. Chen, Y. Lo, and W. Liu, “A 37.6 mm<sup>2</sup> 1024-channel high-compliance-voltage SoC for epiretinal prostheses,” in *Proc. IEEE Int. Solid-State Circuits Conf., Dig. Tech. Papers*, 2013, pp. 294–295.
- [16] H. Gao, R. M. Walker, P. Nuyujukian, K. A. A. Makinwa, K. V. Shenoy, B. Murmann, and T. H. Meng, “HermesE: A 96-channel full data rate direct neural interface in 0.13 um CMOS,” *IEEE J. Solid-State Circuits*, vol. 47, no. 4, pp. 1043–1055, 2012.
- [17] S. F. Liang, F. Z. Shaw, C. P. Young, D. W. Chang, and Y. C. Liao, “A closed-loop brain computer interface for real-time seizure detection and control,” in *Proc. Annu. Int. Conf. IEEE Engineering in Medicine and Biology Soc.*, 2010, pp. 4950–4953.
- [18] F. Shahrokhi, K. Abdelhalim, D. Serletis, P. L. Carlen, and R. Genov, “The 128-channel fully differential digital integrated neural recording and stimulation interface,” *IEEE Trans. Biomed. Circuits Syst.*, vol. 4, no. 3, pp. 149–161, 2010.
- [19] J. D. Rolston, R. E. Gross, and S. M. Potter, “NeuroRighter: Closed-loop multielectrode stimulation and recording for freely moving animals and cell cultures,” in *Proc. IEEE Engineering in Medicine and Biology Soc. Conf.*, 2009, pp. 6489–6492.
- [20] S. Venkatraman, K. Elkabany, J. D. Long, Y. Yimin, and J. M. Carmena, “A system for neural recording and closed-loop intracortical microstimulation in awake rodents,” *IEEE Trans. Biomed. Eng.*, vol. 56, no. 1, pp. 15–22, 2009.
- [21] C. Q. Huang, R. K. Shepherd, P. M. Carter, P. M. Seligman, and B. Tabor, “Electrical stimulation of the auditory nerve: direct current measurement *in vivo*,” *IEEE Trans. Biomed. Eng.*, vol. 46, no. 4, pp. 461–470, Apr. 1999.
- [22] T. Denison, K. Consoer, W. Santa, A. Avestruz, J. Cooley, and A. Kelly, “A 2 W 100 nV/rHz chopper-stabilized instrumentation amplifier for chronic measurement of neural field potentials,” *J. Solid-State Circuits*, vol. 42, no. 12, pp. 2934–2945, 2007.
- [23] Texas Instruments, “MicroPower, single-supply, CMOS instrumentation amplifier,” INA2321 datasheet, Dec. 2000, [Revised Jan. 2006].
- [24] Texas Instruments, “Single-supply, microPower CMOS Op Amp microAmplifier series,” OPA2336 datasheet, Jan. 1997, [Revised Jan. 2005].
- [25] Atmel, AT32UC3C Series Complete Oct. 2010, [Revised Jan. 2012].
- [26] F. Chen, A. P. Chandrakasan, and V. M. Stojanovi, “Design and analysis of a hardware-efficient compressed sensing architecture for data compression in wireless sensors,” *J. Solid-State Circuits*, vol. 47, no. 3, pp. 744–756, Mar. 2012.
- [27] S. Aviyente, “Compressed sensing framework for EEG compression,” in *Proc. 14th Workshop IEEE Statistical Signal Processing*, 2007, pp. 181–184.
- [28] X. Liu, B. Subei, M. Zhang, A. G. Richardson, T. H. Lucas, and J. Van der Spiegel, “The PennBMBI: A general purpose wireless brain-machine-brain interface system for unrestrained animals,” in *Proc. Int. Symp. Circuits and Systems*, 2014.
- [29] Atmel, Atmel 8-bit Microcontroller with 4/8/16/32KBytes In-System Programmable Flash, Sep. 2012, [Revised Feb. 2013].
- [30] Analog Devices, 3-Axis,  $\pm 2g/\pm 4g/\pm 8g/\pm 16g$  digital accelerometer, Jun. 2009, [Revised Feb. 2013].
- [31] Nordic, nRF24L01+ Single Chip 2.4 GHz Transceiver product specification v1.0, Sep. 2008.
- [32] M. Steyaert, W. Sansen, and C. Zhongyuan, “A micropower low-noise monolithic instrumentation amplifier for medical purposes,” *J. Solid-State Circuits*, vol. 22, no. 6, pp. 1163–1168, 1987.



**Xilin Liu** (S'13) received the B.S. degree in electrical engineering from the Harbin Institute of Technology, Harbin, China, and the M.S. degree in electrical engineering from University of Pennsylvania, Philadelphia, PA, USA, in 2011 and 2013, respectively.

Currently, he is working toward the Ph.D. degree at the University of Pennsylvania. His research interests include CMOS image sensors and low power focal-plane signal processing. He is also interested in mixed-signal integrated circuits design for biomedical microsystems, especially for brain-computer interface.

interface.



**Milin Zhang** (S'06–M'11) received the B.S. and M.S. degrees in electronic engineering from Tsinghua University, Beijing, China, in 2004 and 2006, respectively, and the Ph.D. degree from the Electronic and Computer Engineering Department, Hong Kong University of Science and Technology, Clear Water Bay Peninsula, Hong Kong.

Currently, she is a Postdoctoral Researcher at the University of Pennsylvania, Philadelphia, PA, USA. Her research interests include designing traditional and various non-traditional imaging sensors, such as

polarization imaging sensors and focal-plane compressive acquisition image sensors. She is also interested in brain-machine-interface and relative biomedical sensing applications and new sensor designs.



**Basheer Subei** is working toward the B.S. degree in bioengineering (with a neural engineering concentration) at the University of Illinois at Chicago, Chicago, IL, USA.

His research interests include robotics and computer vision using ROS and OpenCV. He is also interested in computational biophysics, machine learning, and high-performance computing.



**Andrew G. Richardson** (M'14) received the B.S.E. degree in biomedical engineering from Case Western Reserve University, Cleveland, OH, USA, in 2000, and the S.M. degree in mechanical engineering and the Ph.D. degree in biomedical engineering from the Massachusetts Institute of Technology (MIT), Cambridge, MA, USA, in 2003 and 2007, respectively.

He was a Postdoctoral Associate at MIT from 2007–2008 and a Senior Fellow at the University of Washington, Seattle, WA, USA, from 2008–2012. Currently, he is Co-Director of the Translational

Neuromodulation Laboratory, Department of Neurosurgery, University of Pennsylvania, Philadelphia, PA, USA. His research interests include neural prostheses for restoring sensory, motor, and memory function.



**Timothy H. Lucas** (M'12) completed neurosurgery and doctoral training in physiology and biophysics at the University of Washington, Seattle, WA, USA, in 2009.

Following training, he had subspecialty fellowships at the University of California, San Francisco, San Francisco, CA, USA. He served as Senior Registrar in the Atkinson Moreley Wing of St. George's Health Care Trust, London, U.K. As Assistant Professor of Neurosurgery, he directs the Translational Neuromodulation Lab and Co-Directs the Center for Neuroengineering and Therapeutics at the University of Pennsylvania, Philadelphia, PA, USA. His research focuses on the developing novel neuromodulation strategies to restore function to patients with paralysis. Clinically, he performs craniotomies for tumor and epilepsy in eloquent brain regions using minimally invasive laser and endoscopic techniques.



**Jan Van der Spiegel** (S'73–M'79–SM'90–F'02) received the Masters degree in electro-mechanical engineering and the Ph.D. degree in electrical engineering from the University of Leuven, Leuven, Belgium, in 1974 and 1979, respectively.

Currently, he is a Professor and Associate Dean for Education of the Electrical and Systems Engineering Department, and the Director of the Center for Sensor Technologies at the University of Pennsylvania, Philadelphia, PA, USA. He is the former chair of the Electrical Engineering and Interim Chair of the Electrical and Systems Engineering Departments. His primary research interests are in mixed-mode VLSI design, CMOS vision sensors for polarization imaging, biologically based image sensors and sensory information processing systems, microsensor technology, and analog-to-digital converters. He is the author of more than 160 journal and conference papers and holds four patents.

Dr. Van der Spiegel was the recipient of the IEEE 2007 EAB Major Educational Innovation Award, the IEEE Third Millennium Medal, the UPS Foundation Distinguished Education Chair, and the Bicentennial Class of 1940 Term Chair. He received the Christian and Mary Lindback Foundation, and the S. Reid Warren Award for Distinguished Teaching, and the Presidential Young Investigator Award. He has served on several IEEE program committees (IEDM, ICCD, ISCAS, and ISSCC) and was the Technical Program Chair of the 2007 International Solid-State Circuit Conference (ISSCC 2007). He is an elected member of the IEEE Solid-State Circuits Society and is also the SCS Chapters Chairs Coordinator and former editor of *North and South America of Sensors and Actuators*. He is a member of Phi Beta Delta and Tau Beta Pi.

Dr. Van der Spiegel was the recipient of the IEEE 2007 EAB Major Educational Innovation Award, the IEEE Third Millennium Medal, the UPS Foundation Distinguished Education Chair, and the Bicentennial Class of 1940 Term Chair. He received the Christian and Mary Lindback Foundation, and the S. Reid Warren Award for Distinguished Teaching, and the Presidential Young Investigator Award. He has served on several IEEE program committees (IEDM, ICCD, ISCAS, and ISSCC) and was the Technical Program Chair of the 2007 International Solid-State Circuit Conference (ISSCC 2007). He is an elected member of the IEEE Solid-State Circuits Society and is also the SCS Chapters Chairs Coordinator and former editor of *North and South America of Sensors and Actuators*. He is a member of Phi Beta Delta and Tau Beta Pi.